20. (Amended) A platform to support one or more semiconductor substrate processing cells, comprising:

a lower mainframe;

an upper mainframe including a plurality of recesses, each one of the plurality of recesses configured to receive a semiconductor substrate processing cell; and

a dampener means disposed between the lower mainframe to the upper mainframe to support the upper mainframe relative to the lower mainframe, wherein the dampener means comprises a dampening element, the dampening element being sand.

21. (Amended) The platform of claim 20, wherein the dampener means comprises a plurality of supporting means that extends between the lower mainframe and the upper mainframe.

REMARKS

This is intended as a full and complete response to the Final Office Action dated December 10, 2002, having a shortened statutory period for response set to expire on March 10, 2003. Claims 1, 8 and 18-21 have been amended to put them in condition for allowance. No new matter has been introduced by the amendments presented herein. The amendments have been made in a good faith effort to advance the prosecution on the merits. Claims 7 and 17 have been cancelled without prejudice. Applicants reserve the right to subsequently take up prosecution of the claims as originally filed in this application or in a continuation, a continuation-in-part and/or a divisional application. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-7, 17-19, and 21 stand rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent No. 2,064,751 (*Hussman*). The Examiner takes the position that the previous amendment to include the "semiconductor substrate processing cell" limitation to the claims has not been deemed persuasive since the limitation has not been positively claimed.

However, in a telephone interview on February 14, 2003, the Examiner agreed that claims 1-6, 8-16 and 18-21 are allowable over the references of record. Applicants appreciate the Examiner's courtesy for scheduling and conducting the interview.

Claims 11-16 are in condition for allowance. Claims 8-10 and 20 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Accordingly, claims 8 and 20 have been rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Claims 8 and 20 are therefore in condition for allowance. Claims 9-10 are also in condition for allowance since they depend from claim 8.

In conclusion, the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the method or apparatus of the present invention. Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

The prior art made of record is noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, it is believed that a detailed discussion of the secondary references is not deemed necessary for a full and complete response to this office action. Accordingly, allowance of the claims is respectfully requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A platform to support one or more semiconductor processing cells, comprising:

a lower mainframe;

an upper mainframe including a plurality of recesses, each one of the plurality of recesses configured to receive a semiconductor substrate processing cell; and

a [dampener system] plurality of supporting members disposed between the lower mainframe and the upper mainframe, wherein each supporting member comprises sand.

8. (Amended) (Allowed) [The platform of claim 7,] A platform to support one or more semiconductor processing cells, comprising:

a lower mainframe;

an upper mainframe including a plurality of recesses, each one of the plurality of recesses configured to receive a semiconductor substrate processing cell; and

a plurality of support members between the lower mainframe and the upper mainframe, wherein each support member comprises:

a hollow tubular member;

a piston slidably disposed within the hollow tubular member; and

a dampening element contained within the hollow tubular member, wherein the piston is biased against the dampening element.

18. (Amended) The platform of claim [17] 20, wherein the upper mainframe further comprises a fastener means positioned proximate each one of the recesses, wherein the fastener means is configured to hold the semiconductor substrate processing cell.

19. (Amended) The platform of claim [17] 20, wherein the upper mainframe further comprises a rigidifying plate and a main base plate comprising the plurality of recesses, the rigidifying plate comprising at least one aperture and attached to the main base plate such that the at least one aperture is aligned with the recesses.

20. (Amended) [The platform of claim 17] A platform to support one or more semiconductor substrate processing cells, comprising:

a lower mainframe;

an upper mainframe including a plurality of recesses, each one of the plurality of recesses configured to receive a semiconductor substrate processing cell; and

a dampener means disposed between the lower mainframe to the upper mainframe to support the upper mainframe relative to the lower mainframe, wherein the dampener means comprises a dampening element, the dampening element being sand.

21. (Amended) The platform of claim [17] 20, wherein the dampener means comprises a plurality of supporting means that extends between the lower mainframe and the upper mainframe.